7 Segment Decoder

Javier Mondragón Martin del Campo

Laboratory exercise number:

Lab. 01

Laboratory exercise name:

Binary 7 Segment Decoder

|  |  |  |
| --- | --- | --- |
| Names: | Roll Number | Date |
| Javier Mondragón M. | A01365137 | 30/August/2019 |

Lab description:

The purpose of this laboratory is to learn how program an FPGA using VHDL with the architecture “dataflow” using the skills learnt in class.

The material used was:

Nexys 3 by Digilent for the FPGA

ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

Schematics, block diagrams and/or timing diagrams:

Using the following truth of table I wrote the code displayed in the image 1.1.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D | C | B | A | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

Image 1.1

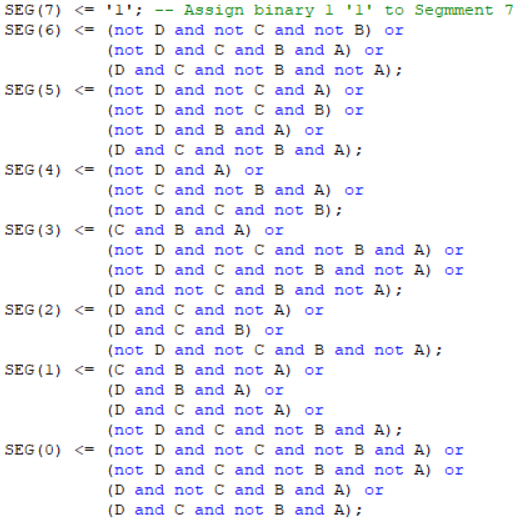


Image from code with equations

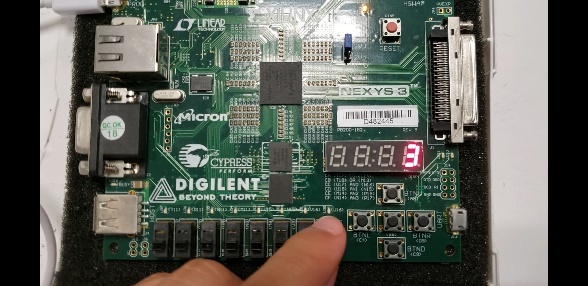
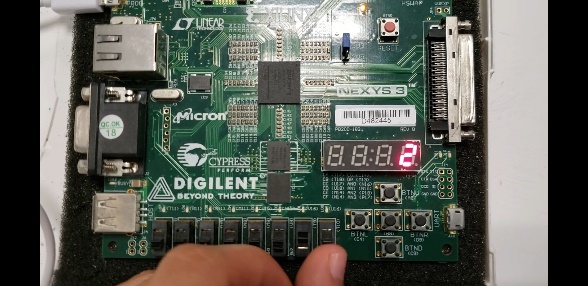
Results obtained:

The result was a successful decoder from binary to digital displayed in the FPGA using also the switches and 7 segment display as input and output.

Evidence:

<https://youtu.be/rG0PHXEaRsk>

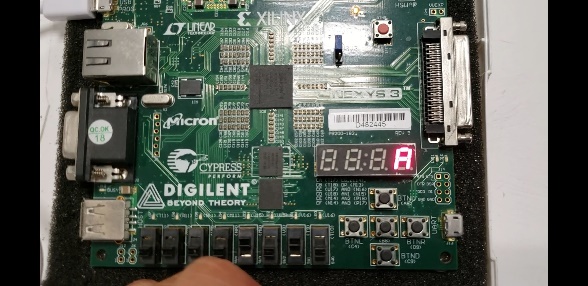
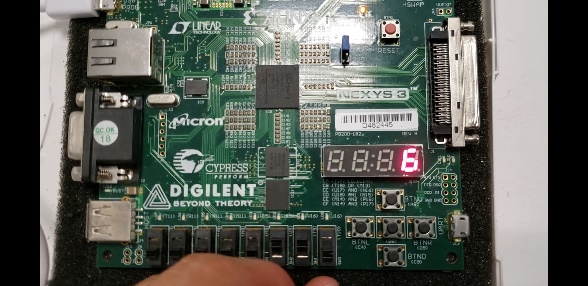
Case 1 Case 2



Case 3 Case 4



Case 5 Case 6



Conclusions:

The FPGA is an artefact to simplify the prototyping and do it much faster. It could be used to test circuits and correct it much easier and faster.

Problems encountered:

These were pretty much with the FPGA and the pins, because I didn’t have the right program to write down the pinout, downloading and installing was tedious but made the process much faster. Obtaining the equations there also got time but there wasn’t any difficulty at all.